

**FIG. 1** 

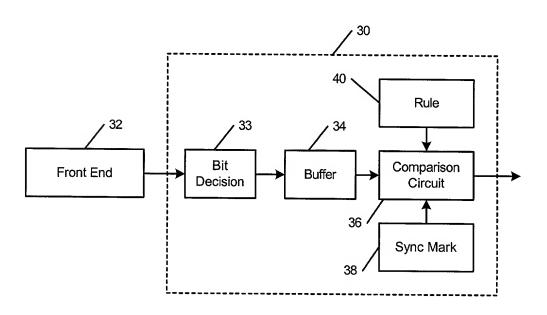


FIG. 2 Prior Art

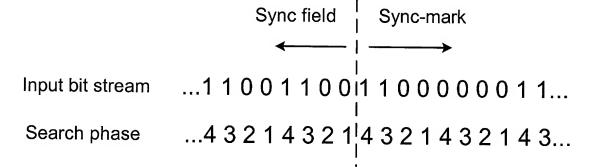
**FIG. 3** 

Input 110011001100000011

Error-event 0000-000000000000

Output 110001001100000011

**FIG. 4** 



**FIG. 5** 

NRZ Domain	INRZI Domain			
+-+	xx0xx			
+	x0x			
+-	XXXX			
+00+	x0xx0x			
+000+	x0x0x0x			
+0+	x000x			

Most Likely Error-Events

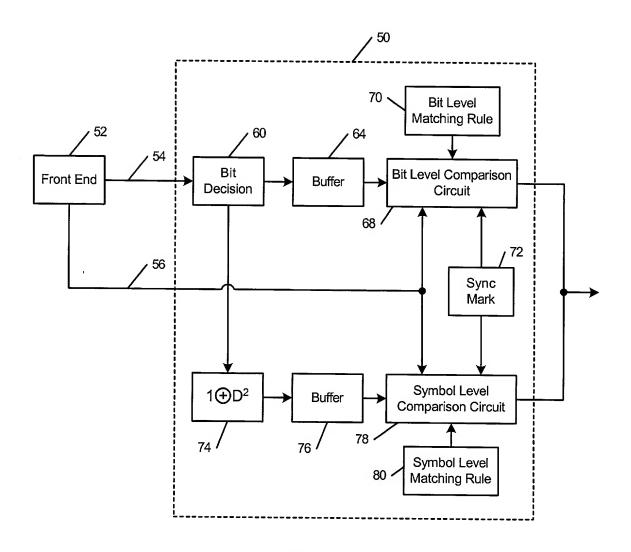


FIG. 6A

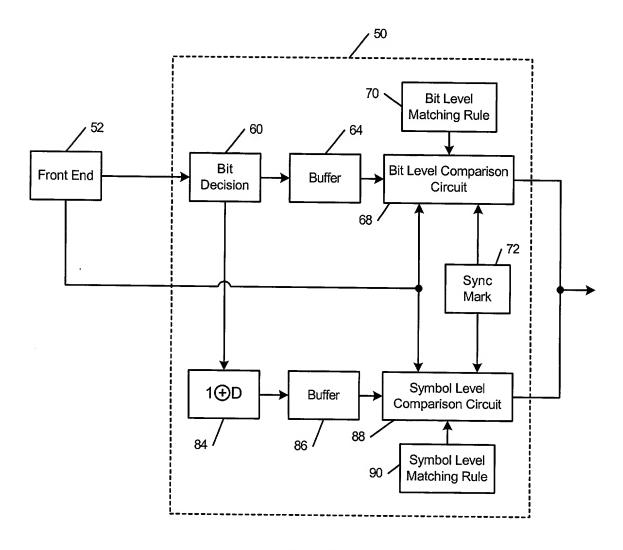
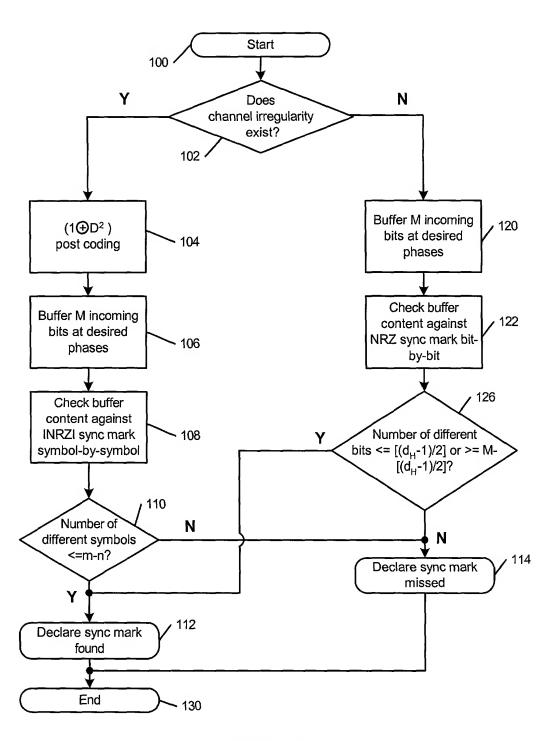


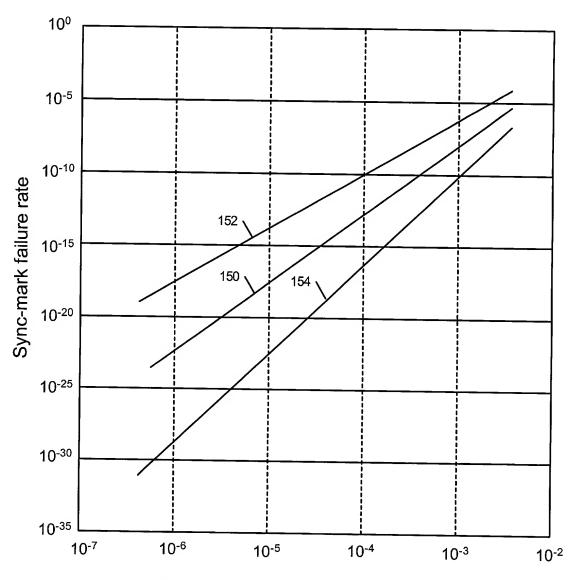
FIG. 6B

Sync-mark	bbbbb	bbbbb	bbbbb	bbbbb	bbbbb	bbbbb	bbbbbb
NRZ Error-Event	+	00+					
INRZI Error-Event	x	0xx0x					

FIG. 7



**FIG. 8** 



Bit error rate at the input to the syncmark detector

FIG. 9